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RECORD OF ORAL HEARING

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

EX PARTE SUNG-KYU CHOI

Appeal 2008-4828
Application 10/758,040
Technology Center 2100

Oral Hearing Held: February 11, 2009

Before JOHN C. MARTIN, JEAN R. HOMERE, and CAROLYN D. THOMAS, *Administrative Patent Judges.*

APPEARANCES:

ON BEHALF OF THE APPELLANT:

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The above-entitled matter came on for oral hearing on Wednesday, February 11, 2009, at The U.S. Patent and Trademark Office, 600 Dulany Street, Alexandria, Virginia, before Lorie B. Allen, Notary Public.

JUDGE MARTIN: You can proceed whenever you are ready.

MR. WALLERSON: Good morning again, Your Honors.

I'd first like to take a look at claim one. The basis of claim one -- there are four independent claims. I'd like to first focus on claim one.

The major contention that we have is that the two cited references, Bourke and Barrenscheen, acknowledged by the Examiner, Bourke does not disclose a multiplexer, the last element of the claim, wherein the multiplexer receives first data from the processor and transfers the received first data, the first memory, through a synchronous data bus, synchronized with the processor, or receives second data from the first memory through a synchronous data bus and transfers the second data to a processor.

The Examiner cites Barrenscheen as disclosing that cited limitation. Apparently uses the bus interface BI1 in Figure 4 as allegedly reading on the claimed multiplexer.

Our position is that the bus interface cannot be construed as being a multiplexer. There is no disclosure in the cited reference that that bus interface could be used in any way as a multiplexer.

Further, we don't believe that bus one and bus two, which the Examiner appears to assert, on the synchronous bus and asynchronous bus could be construed as being synchronous and asynchronous buses. There is

no disclosure in the references that either one of those buses, either synchronous or asynchronous --

JUDGE HOMERE: Counsel, let's go over your arguments one by one. Let's start with the argument regarding the multiplexer. It calls for a multiplexer that receives data and transfers data; right?

MR. WALLERSON: Correct.

JUDGE HOMERE: The Examiner's position is that the interface, the bus interface, performs these same functions because it enables the data transfer unit to receive data from one of the modules and then to transfer it to another module.

Technically, would you agree this bus interface at least performs these two functions, the function of receiving and transferring the data?

MR. WALLERSON: Maybe in terms of receiving one stream of data and transferring that single stream, but there is no disclosure in the reference that that bus interface may receive multiple streams and then multiplex that into single streams of transfers to a bus.

JUDGE HOMERE: Does the claim require that the received data is multiplexed before it is transferred? All you have is the nominal term of a "multiplexer." Functions specific to the multiplexer being performed by the multiplexer.

Really, for that matter, you could have any device that's capable of transferring the data. You do agree that this bus interface performs the same functions except you are alleging that for certain functions that are not claimed, cited in the claim, are not being performed by the bus interface.

MR. WALLERSON: I would agree with that but also even if you considered the bus interface to be a multiplexer, there is no disclosure in the reference that that bus interface transfers data through a synchronous bus to a first memory, and also there is no disclosure of asynchronous parts of the claim.

JUDGE HOMERE: All right. You are conceding the argument regarding the multiplexer. Now we are going to the synchronous limitation--

MR. WALLERSON: Correct.

JUDGE HOMERE: How do you define "synchronous" and "asynchronous?" What is the meaning of those terms?

MR. WALLERSON: "Synchronous" means -- well, as disclosed by the specification, "synchronous" would mean that that bus is synchronized with a processor clock-wise.

JUDGE HOMERE: Can you expand on that a bit more? What does that mean, that the bus is synchronized with the processor?

MR. WALLERSON: The data on the synchronized bus is programmed to send data based on certain clock signals, as opposed to the asynchronous bus, where the data is stored in a buffer prior to being sent to the asynchronous bus, so it's not really synchronized or sent in the same time based on the processor.

JUDGE MARTIN: Is it fair to say that although the processor is connected to the asynchronous bus and the synchronous bus, it only controls the synchronous bus?

MR. WALLERSON: It only controls the synchronous bus.

JUDGE MARTIN: But it can still send information back and forth on the asynchronous bus?

MR. WALLERSON: Through the buffer.

JUDGE MARTIN: The asynchronous bus, that's just not --

MR. WALLERSON: The data is first sent to a buffer as shown in Figure 2 of the current invention. The data is sent to a buffer, to a multiplexer, then to a buffer, and then sent to the second memory on the asynchronous bus.

It is not synchronized with the processor as opposed to the synchronized bus which is synchronized with the processor.

We don't see those limitations being shown in any of the cited references, especially claim one, the Examiner uses Bourke and Barrenscheen for those limitations.

JUDGE MARTIN: I wonder if you could tell me a little bit more about our primary reference, Bourke. Doesn't the Examiner read the term "multiplexer" on that interface 14 in Figure 2-A? He does call that a "multiplexer," right?

I'm looking at the Answer, page three, halfway down, that last paragraph, the line beginning "I.e., instruction processor, Unit 10A of Figure 1, is provided by a multiplexer," and then in parentheses "i.e. adapter interface 14 of Figure 2-A."

I guess what I'm getting at is what's missing? Is it wrong to call that a multiplexer or is it not functioning in the way that the claim requires the multiplexer to function?

MR. WALLERSON: That's our point. We don't believe that even if those are construed to be multiplexers, there is no disclosure. The crux of the invention is sending data, to connect the processor to two different buses, one synchronized and the other asynchronous, where with the asynchronous transfer of data, it is sent to a multiplexer and then sent to a buffer prior to being sent to the asynchronous bus.

I'm sorry. Correct, sent to a buffer prior to being sent to the asynchronous bus.

There is no disclosure. Even if those elements may be construed to be multiplexers, which we don't admit, there is no disclosure that data is being sent to asynchronous buses or synchronous buses through a multiplexer, through either of these elements.

JUDGE MARTIN: I'm sorry, counsel. I'm losing you on this argument. In Figure 2-A, interface 14 is called by the Examiner a multiplexer, and it has an adapter bus on one side that's synchronous, I believe, it's described that way in the reference, and on the other side of this interface, you have the SPD bus, which is described as asynchronous.

You have this multiplexer that's between an asynchronous bus and a synchronous bus or you have this interface 14 anyway, that is between an asynchronous bus and a synchronous bus. Is that correct?

MR. WALLERSON: We have two interface 14s.

JUDGE MARTIN: He called the whole thing 14. Okay. There are three parts to that, aren't there. I don't know what you call that whole block. He has called the upper adapter interface -- the reference refers to that as 14, and the SPD bus interface is 12.

I see. The whole block is one of 10J, 10K, 10L, et cetera.

The Examiner, he was reading the claim, multiplexer, on just the adapter interface 14, I guess.

JUDGE HOMERE: If you go to Figure 1, you have the SPD bus, which is the synchronous bus. You have the IOICs, which is the input/output interface controllers. The input/output interface controllers, this is what the Examiner construed as being the multiplexer, and on the other side, you have the adapter bus.

The input/output interface controller is better described in Figure 2 where it says it is comprised of a register and a variety of logic in there.

I guess the question that Judge Martin was asking was if the input/output interface controller is the multiplexer and then you have the asynchronous and synchronous buses, why would that not be -- how would that be different from the current invention.

MR. WALLERSON: You still don't show any disclosure that the data is being sent -- in terms of how the claim is drafted -- we have the multiplexer that receives data from a first processor. That data is then sent to a first memory through a synchronous bus.

The Examiner acknowledges that Bourke does not teach those parts, those elements of the claim. Even if 14 is construed as being a multiplexer, even the combination of Bourke and Barrenscheen do not disclose those elements of a multiplexer receiving data from a processor, transferring that data to a first memory through a synchronous bus.

JUDGE HOMERE: The argument here is we at least have come to a preliminary agreement that the interface performed the function of the

multiplexer, so in Bourke, you have an asynchronous bus and a synchronous bus, and then you have the interface that sits between them that enables one to transfer data out from the synchronous bus or to the asynchronous bus.

Now, when you turn to Barrenscheen, this is the interface that enables you to transfer data between a first module and a second module. I think this is how the Examiner is trying to patch -- combine the references.

Technically, if you look at Figure 2 of Barrenscheen, you have the first module that can be a computer or storage media, so you can send data --

MR. WALLERSON: I'm sorry. Figure 2?

JUDGE HOMERE: Figure 2-A of Barrenscheen.

If you send data from the first module over to that bus --

MR. WALLERSON: The first module being BU11?

JUDGE HOMERE: B11, this module can be a computer or a storage media. Let's say it's a computer. You have a computer sending first data to the interface, the interface receiving the data, transferring the data to the second module via the bus, the first bus. That would read exactly on the claim.

MR. WALLERSON: There is no disclosure that --

JUDGE HOMERE: The other thing that's missing here is the synchronous limitation, that bus is synchronized to the computer.

MR. WALLERSON: Right; correct.

JUDGE HOMERE: If we go back to Bourke, because Bourke teaches a synchronized bus and an asynchronized bus and having in between them an interface.

I don't understand why the Examiner would not be able to rely on Bourke for that limitation. In other words, having an interface that's capable of transferring data to a synchronous bus. Unless you raise the argument that the computer is not synchronized, the bus is not synchronized, the bus in Bourke.

MR. WALLERSON: In Bourke; exactly.

JUDGE HOMERE: Don't let me put words in your mouth.

MR. WALLERSON: No. Right. That's an adapter bus. There is no teaching that bus is synchronized with a processor.

JUDGE HOMERE: When you look at the disclosure of Bourke, it says that the adapter bus is a synchronized bus, and the SPD bus is an asynchronous bus. It's right there in column one and two.

You do have an interface that's interfacing, in other words, transferring data between a synchronized bus and a computer.

MR. WALLERSON: There's no motivation to combine those references in any case. There is no teaching in Barrenscheen that bus one or bus two are synchronized or asynchronous in any way.

JUDGE HOMERE: There is synchronized teaching in Bourke. Really, all you need Barrenscheen for is for the claimed structure. That is all Barrenscheen provides you with is the ability to get data from a first computer and transfer it over to a storage media via the interface, and vice versa.

Really, the ability to send a first data and a second data over to the other side via the interface and the bus.

Really, what is missing in Barrenscheen is the bus being synchronized with the computer, the processor, but you have that teaching in Bourke.

Really, the bottom line is if it would have been much better to combine these two here.

MR. WALLERSON: Our argument is one would not have been motivated to combine those references.

JUDGE HOMERE: Why not?

MR. WALLERSON: We think the motivation would have to be in the secondary reference, Barrenscheen.

JUDGE HOMERE: In the secondary reference? Why? Why could it not be in the primary reference? What is the support, what is the legal support for that?

You're familiar with KSR?

MR. WALLERSON: Yes.

JUDGE HOMERE: Someone who is not an attorney, someone who is a competent person who is able to use common knowledge in order to come up with a reasonable combination.

From putting these two references together -- I have the interface in both references and then I have a synchronized bus and an asynchronized bus, and I'm transferring data between a processor and a memory, therefore, I have the invention.

MR. WALLERSON: In terms of the first and second memories, there is no teaching that the data is being transferred -- well, even if you construe the modules, there is no teaching that the data is being transferred to first and second memories on those buses. I mean the modules --

JUDGE HOMERE: What do you mean? You have a bi-directional transfer of data between the two modules.

MR. WALLERSON: You are construing the DTU, the data transfer unit, as being the multiplexer.

JUDGE HOMERE: DTU; yes. The bus interface inside the data transfer unit is the multiplexer, which is already provided in Bourke as the input/output interface controller.

MR. WALLERSON: There is no teaching that interface has a memory, a buffer, that can store the data prior to it being sent to a synchronous bus.

JUDGE HOMERE: Yes, it does. Figure 2 of Bourke, the interface, input/output interface controller 20, it has registers and buffers in it.

MR. WALLERSON: All right. The second rejection of claims two, four and ten.

JUDGE MARTIN: Go right ahead.

MR. WALLERSON: A difference reference for claims two, four and ten, Masayuki. We believe the same argument would also apply in this case with regard to Masayuki.

We do not believe that Masayuki discloses the synchronized and asynchronized buses. The Examiner cited Figure 3 and buses 33 and 34 as allegedly reading on the synchronous and asynchronous buses, respectively.

There is no disclosure that bus 34 is synchronized or synchronous with a processor. There is no disclosure that bus 33 is asynchronous.

JUDGE HOMERE: Let me read the Examiner's position regarding Masayuki. The Examiner says that -- Figure 2 -- the Examiner says --

MR. WALLERSON: Figure 2 of Masayuki?

JUDGE HOMERE: Of Masayuki. The Examiner says the image data bus, you are able to transfer data between the CCD sensor to the outside memory unit, which is the image memory unit, item 32, via the asynchronous bus.

The Examiner alleged that the image data bus is an asynchronous bus and the CPU data bus is a synchronous bus.

MR. WALLERSON: We believe the Examiner is reciting subject matter that is not taught or suggested by the claim, by the reference. There is no teaching of those assertions in the reference.

JUDGE HOMERE: What do you think about -- when you look at Figure 1, there is the sync generator that sends a signal to the image generator unit, and then the image generator unit sends back synchronized components. I'm referring to generator 26 that sends a signal.

Does this have anything to do with processor 20 being synchronized with the image generator 10?

MR. WALLERSON: Correct.

JUDGE HOMERE: Do you see what I'm talking about?

MR. WALLERSON: Yes.

JUDGE HOMERE: 26 in Figure 20, a sync generator, sending a sync signal to the image generator, which is 10. The image generator in return is sending a signal back to the image processor, and that goes into the memory controller 22 that distributes all the other signals to the other components in the system.

MR. WALLERSON: I'm not sure how you're reading the asynchronous aspect of that, by bus 33 being asynchronous, because they seem to be connected -- those buses are connected together.

JUDGE HOMERE: Okay. You have a sent signal. The Examiner is saying at least if you are assuming the sent signal that you're getting in there goes through -- that's the same signal that's being fed to that bus, right, bus 33, that bus with respect to the image sensor would be de-synchronous.

MR. WALLERSON: They are both de-synchronous.

JUDGE HOMERE: The input, the CCD, I'm looking at Figure 2, CCD and the image data bus, that would be synchronous to that bus. However, when you look at CPU 41, that is connected to the CPU data bus, the Examiner said that the way you communicate, that CPU communicates with the image data bus is through three different interfaces.

MR. WALLERSON: We don't believe that. We believe they are connected -- there is one connection between 33 and 34, between bus 33 and bus 34.

JUDGE HOMERE: You have more than one connection. You have that line, that direct line, 33 and 34. You have a JPEG Kodak 29 that connects them together.

Really, the Examiner used the term "inherent."

MR. WALLERSON: Inherent; yes.

JUDGE HOMERE: The Examiner says those terms, "synchronous" and "asynchronous" are not disclosed in this reference, but one of ordinary skill in the art would know that, according to that configuration there.

MR. WALLERSON: That's the problem that we have. We don't believe that inherency would actually work in this aspect, in this case. That is reading subject matter into the reference that is distinctly not there.

JUDGE HOMERE: Okay.

JUDGE MARTIN: Do you have anything else?

MR. WALLERSON: No, sir.

JUDGE MARTIN: Thank you, counsel. We'll take the case under advisement.

MR. WALLERSON: Thank you very much.

(Whereupon, the proceedings were concluded on February 11, 2009.)